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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Troutman et al.

Assignee: ZiLOG, Inc.

Title: "Architecture to Relax Memory Performance Requirements"

Serial No.: 10/658,058 Filed: September 8, 2003

Patent No.: 6,970,993 B2 Issued: November 29, 2005

Examiner: Woo H. Choi Group Art Unit: 2189

Atty. Doc. No.: ZIL-244-1C

December 4, 2005

ATTN: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Pursuant to 37 CFR 1.322, Applicants request that the Director issue a certificate of correction to correct mistakes in the printing of the above-identified patent incurred through the fault of the Patent Office. Mistakes in the printing of claims 7-8 and 10-11 are clearly apparent when the attached page of USP 6,970,993 (marked to show the mistakes) is compared to the five attached pages of the Listing of Claims that were submitted on June 27, 2005, along with an RCE and an amendment in response to the last office action.

The mistakes relate to the numbered references to base claims upon which dependent claims 7-8 and 10-11 depend. In printing, the final claim numbers were obtained from the following original claim numbers:

1 <= 10	6 <= 27	11 <= 39	16 <= 34
2 <= 31	7 <= 28	12 <= 40	17 <= 35
3 <= 32	8 <= 29	13 <= 33	18 <= 36
4 <= 25	9 <= 30	14 <= 41	19 <= 37
5 <= 26	10 <= 38	15 <= 42	

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Patent No.: 6,970,993 B2
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The attached Listing of Claims shows that (i) claim 28 depends from claim 26, (ii) claim 29 depends from claim 25, (iii) claim 38 depends from claim 27, and (iv) claim 39 depends from claim 27. Thus, in the final claim numbers, (i) claim 7 should depend from claim 5, (ii) claim 8 should depend from claim 4, (iii) claim 10 should depend from claim 6, and (iv) claim 11 should depend from claim 6.

Text of the requested correction is submitted on the one attached page of Certificate of Correction form, PTO/SB/44.

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Date of Deposit: December 4, 2005

Respectfully submitted,

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could latch that address information to make it constantly available to the memory for States 3,4,0. The OTP data would be evaluated during that time period and be available for loading into the op-code latches at the end of State 0.

As only a single memory fetch is used for a 3-byte instruction is this architecture, the demands placed on the memory are greatly reduced. For example, in a arrangement such as in FIG. 1, this will allow a 5× relaxation in the memory access times compared to an implementation needing two fetches. This relaxation can be used to prolong the usable life of an existing technology or utilized by modifying the memory designs to either use lower power, smaller silicon area, lower voltage operation, or adding more memory while maintaining current performance. Alternately, or it can be used to increase device speed independently of clock rate. Again referring to FIG. 1, the use of a single, 24-bit instruction fetch frees up a time slot. Consequently, the device could be reduced from a 5-state operation to 4 states, improving instruction execution times by 20%.

The described structure generalizes in a number of ways. As already mentioned, its use in an OTP memory is just an exemplary embodiment. The described methods and structure can be used with any memory to supply data along a three byte wide bus. Additionally, the choice of the width of 3-bytes is only one example.

In a more general embodiment, the memory can consist of 2N subdivisions of the memory, each K bits wide, with a data bus (N+1)×K bits wide. In the exemplary embodiment, N=2 so that the 2N subdivisions are OTP3-OTP0, and K=8, so that the data bus is three bytes wide. As address structures are generally binary based, the structure of FIG. 4 is most readily implemented when $N=2^n$. In any of these cases, the instructions or other data can be stored contiguously so that no memory space is wasted, even though the width of the bus and the number of columns in the memory are relatively prime, and still supply an instruction the full width of the bus in a single fetch. To use supply M byte wide instructions, where M is still between N and 2N but not equal (N+1), would require the division of the memory into more than two sub-memories and additional multiplex circuits such as 423 of FIG. 4.

For example, consider the case of 5-byte instructions. The memory would then consist of eight memory columns, or OTP7-OTP0, which are split into Memory #1 of OTP7-OTP4 and Memory #2 of OTP3-OTP0. Which of these memories a byte lives in is determined by RMAL[2], which is consequently supplied to the multiplex circuit corresponding to 423 of FIG. 4. The full address is again supplied to Memory #1. When RMAL[2]*=1, the multiplex supplies the full address to Memory #2. As the row is specified by RMAL[R:3], where R is the number of rows, when RMAL [2]=1, RMAL[R:3] plus one is supplied to Memory #2.

Although the various aspects of the present invention have been described with respect to specific exemplary embodiments, it will be understood that the invention is entitled to protection within the full scope of the appended claims.

What is claimed is:

1. A microprocessor, comprising:

a central processing unit with an instruction set including three-byte instructions, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein all of a selected set of the instructions is stored contiguously without any gaps; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said selected instructions are supplied simultaneously in a single fetch operation.

2. The microprocessor of claim 1, wherein said memory is four bytes wide.

3. The microprocessor of claim 1, wherein said memory is a one time programmable memory.

4. A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M byte-wide columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming a selected set of instructions of the instruction set into the memory, wherein all of the selected set of instructions is stored contiguously without any gaps in the memory; and

operating the interface whereby each of the selected instructions can be supplied simultaneously from the memory to the central processing unit in a single fetch operation.

5. The method of claim 4, wherein N is equal to three and M is equal to four.

6. The method of claim 5, wherein said instruction set further includes two byte instructions and one byte instructions.

7. The method of claim 5, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

8. The method of claim 4, wherein the memory is an embedded memory of the microprocessor.

9. The method of claim 8, wherein the memory is a one time programmable memory.

10. The method of claim 5, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

11. The method of claim 4, wherein the memory is an embedded memory of the microprocessor.

12. The method of claim 11, wherein the memory is a one time programmable memory.

13. A microprocessor, comprising:

a central processing unit with an instruction set including three-byte instructions, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions are supplied simultaneously in a single fetch operation, and wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

14. The microprocessor of claim 13, wherein the memory is an embedded memory of the microprocessor.

15. The microprocessor of claim 13, wherein the memory is a one time programmable memory.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Bruce L. Troutman et al.		
Title:	Architecture to Relax Memory Performance Requirements		
Application No.:	10/658,058	Filing Date:	September 8, 2003
Examiner:	Woo H. Choi	Group Art Unit:	2186
Docket No.:	ZILG.244US1	Conf. No.:	5500

Certificate of Mailing Under 37 CFR 1.8

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Signature Eileen Bowen

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P.O. Box 1450
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AMENDMENT

Dear Sir:

This Amendment is responsive to the Official Action mailed on January 25, 2005, and for which a two-month extension is hereby requested. Applicant responds to the Official Action as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

Claims 10, 11, 25, 28, 31, 33, 34, and 38 have been amended, claims 9 and 12 have been cancelled, and new claims 41 and 42 have been added. This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

(Claims 1-9 have been cancelled)

10.(Currently Amended) A ~~The~~ microprocessor ~~of claim 9~~, comprising:

a central processing unit with an instruction set including three-byte instructions~~wherein said instruction set further includes~~, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein all of a selected set of the instructions is stored contiguously without any gaps; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said selected instructions are supplied simultaneously in a single fetch operation.

11.(Currently Amended) ~~The~~ microprocessor ~~of claim 9~~, comprising:

a central processing unit with an instruction set including three-byte instructions;

a memory for storing the instructions, wherein all of a selected set of the instructions is stored contiguously without any gaps; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said selected instructions are supplied simultaneously in a single fetch operation, and wherein said memory is a one time programmable memory.

(Claims 12-24 have been cancelled)

25.(Currently Amended) A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a memory interface for supplying the

instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M byte-wide columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming a selected set of instructions of the instruction set into the memory, wherein all of the selected set of instructions ~~are~~ is stored contiguously without any gaps in the memory; and

operating the interface whereby each of the selected instructions can be supplied simultaneously from the memory to the central processing unit in a single fetch operation.

26.(Previously Presented) The method of claim 25, wherein N is equal to three and M is equal to four.

27.(Previously Presented) The method of claim 26, wherein said instruction set further includes two byte instructions and one byte instructions.

28.(Currently Amended) The method of claim 26, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

29.(Previously Presented) The method of claim 25, wherein the memory is an embedded memory of the microprocessor.

30.(Previously Presented) The method of claim 29, wherein the memory is a one time programmable memory.

31(Currently Amended) The microprocessor of claim 10, wherein said memory is four bytes wide.

32.(Previously Presented) The microprocessor of claim 10, wherein said memory is a one time programmable memory.

33.(Currently Amended) A ~~The~~ microprocessor ~~of claim 10~~, comprising:

a central processing unit with an instruction set including three-byte instructions, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions are supplied simultaneously in a single fetch operation, and wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

34.(Currently Amended) A microprocessor, comprising:

a central processing unit operable according to an instruction set including instructions of one-byte, two-byte, and three-byte lengths;

a memory for storing a selected set of said instructions, wherein all of the selected ~~members of the instruction~~ set ~~are~~ is stored contiguously without any gaps; and

a memory interface for supplying instructions of the instruction set from the memory to the central processing unit, wherein each of said instructions is individually suppliable in a single fetch operation in which all bytes of a supplied instruction are supplied simultaneously.

35.(Previously Presented) The microprocessor of claim 34, wherein said memory is organized as a plurality rows of M byte-wide columns, wherein M is an integer greater than three that is not divisible by three.

36.(Previously Presented) The microprocessor of claim 34, wherein said memory is a one time programmable memory.

37.(Previously Presented) The microprocessor of claim 34, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

38.(Currently Amended) The method of claim 27, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

39.(Previously Presented) The method of claim 27, wherein the memory is an embedded memory of the microprocessor.

40.(Previously Presented) The method of claim 39, wherein the memory is a one time programmable memory.

41.(New) The microprocessor of claim 33, wherein the memory is an embedded memory of the microprocessor.

42.(New) The microprocessor of claim 33, wherein the memory is a one time programmable memory.

PTO/SB/44 (04-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,970,993 B2

APPLICATION NO.: 10/658,058

ISSUE DATE : November 29, 2005

INVENTOR(S) : Troutman et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8, lines 30, 34, 38 and 42, claim dependency numbers should be corrected as follows: (i) claim 7 should depend from claim 5, (ii) claim 8 should depend from claim 4, (iii) claim 10 should depend from claim 6, and (iv) claim 11 should depend from claim 6.

Lines 30-43, claims 7-11 should read:

7. The method of claim 5, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

8. The method of claim 4, wherein the memory is an embedded memory of the microprocessor.

9. The method of claim 8, wherein the memory is a one time programmable memory.

10. The method of claim 6, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

11. The method of claim 6, wherein the memory is an embedded memory of the microprocessor.

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